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Institute of Technology

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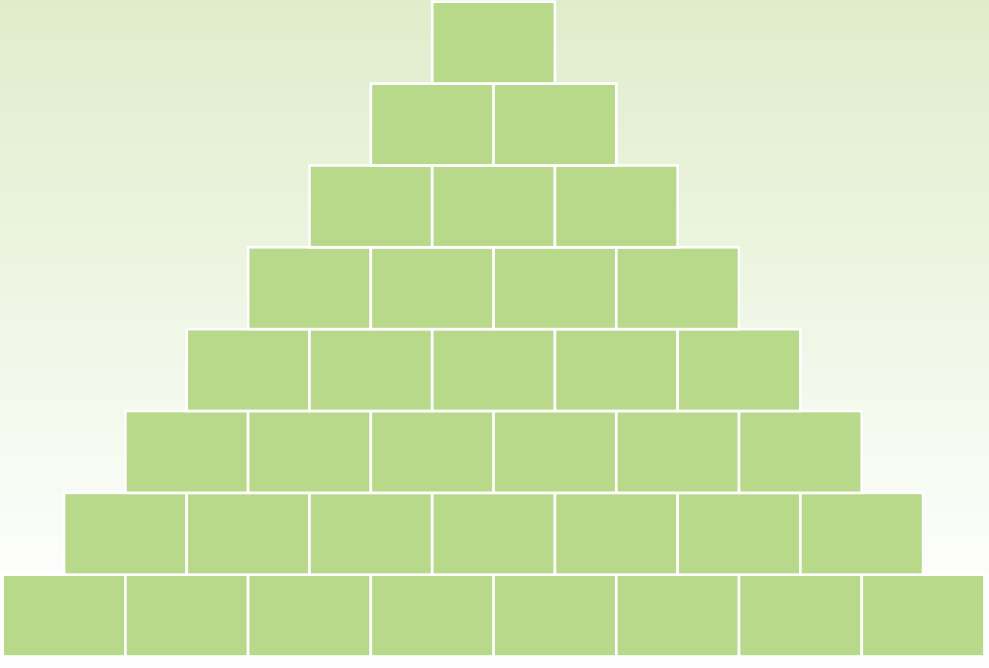
2010-11



Placements

VIGNANA BHARATHI INSTITUTE OF TECHNOLOGY

CSS CORP CAMPUS DRIVE ON 20th Feb 2011

VIGNANA BHARATHI INSTITUTE OF TECHNOLOGY

HCL Tech. CAMPUS DRIVE ON 27th Feb 2011

FOREWORD

Projects. vbit present project ideas and abstracts with the best of its selected quality.

The collection of ideas and abstracts of students are compiled by experts in the college. Every year, it is expected to have more and more projects to be added into the system. Students capture the latest technology trends in the market and create projects based on that.

Engineering requires men and women of imagination who can plan and create. The engineer's resources include an intimate knowledge of scientific laws and their applications to engineering problems. An ability to use mathematics and computers and, above all, an imaginative and an inquiring mind are primary tools in an engineer's toolbox.

Students do not devote their attention solely to innovations in technology. They look beyond their inventions and conceptions to consider the societal effect of their work, including its economic, aesthetic, safety, and environmental aspects.

Engineers can start their careers in many functional roles - designer, test engineer, manufacturing engineer, sales engineer, researcher, or a combination of these and other roles. Engineering has become a profession that often leads to executive management positions. As more and more of the decisions of management in government and business are based on technical considerations, engineers with the necessary background are called upon to make these choices.

For all engineers, continuing professional competence in the midst of our constantly changing technology requires educational renewal and a life-long dedication to continuing education. The College offers seminars, institutes and off-campus programs designed to meet this need. In addition, regular college courses are available on an elective, post-degree basis. .

The evolution of our civilization has always been closely associated with technology and science. Now, and in the future, this association will become even more important. New knowledge has inspired advances in technology, resulting in new career opportunities. Far-reaching developments have been made in communications and instrumentation technology. Highly sophisticated machine tools and manufacturing processes have come into being. New energy sources and new man-made materials have been developed, and computer applications have revolutionized the techniques of industrial manufacturing and management.

Because of the increasing challenges in this information age, it is no longer possible for one person to master all of the knowledge and skills necessary to execute technical projects. Quite often, a team effort is required -- with each member of the team highly trained in a specific area. Today's engineering teams involve engineers and engineering technologists and may also include technicians, scientists, physicians, craftsmen, and other specialists.

Engineering technology supports engineering activities through a combination of scientific and professional knowledge with technological skills and concentrates on the industrial applications of engineering. Because of the extensive variety of functional opportunities, and the wide variety of industrial enterprises available to the engineering technologist, there has been a great deal of specialization. An engineering technologist can specialize in three related ways: discipline, function and industry. For example, the discipline could be mechanical, the function could be design, and the industry could be automotive; or the discipline could be electrical, the function field installation, and the industry electric power generation. Through its undergraduate and graduate programs, the four years of engineering study allows students to gain the specialization that they desire to contribute to interdisciplinary teams as engineering technologists.

At VBIT students are encouraged to develop research orientation since the first year of engineering through a technical seminar competition, Avishkar. Hands-on research experience provides important preparation for graduate school as well as professional opportunities.

This book, projects.vbit, showcases the VBIT's selected undergraduate research projects and allows student researchers the opportunity to share their work through panel and presentations. Students begin working on a career plan the day they enter the Institute which culminates in year four when they do a project. This represents the summation of their undergraduate work and is the first step toward a postgraduate career.

VBIT graduates are better prepared by virtue of the career-building experiences beginning with the freshman seminar including undergraduate research projects, and faculty mentoring .These experiences are beneficial in applying for jobs, as well as graduate or professional study.

-Prof. D.Padmawathi

H.O.D, EEE & Editor I/c

-Dr.Jayant Kulkarni,

I/c Principal

VIGNANA BHRATHI INSTITUTE OF TECHNOLOGY

AUSPAHPUR, GHATKESAR, R R DIST.

B.TECH SELECTED PROJECT DURING THE ACADEMIC YEAR 2010 -2011

DEPARTMENT OF ELECTONICS AND COMMUNICATION ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

DEPARTMENT OF INFORMATION TECHNOLOGY

DEPARTMENT OF ELECTONICS AND COMMUNICATION ENGINEERING

REMOTE I/O DATA ACQUISITION SYSTEM BASED ON EMBEDDED ARM

Kalagotla Pitchaiah, G. Pavan, Sheshadri A.V

Abstract

With the rapid development of the field of industrial process control and the fast popularization of embedded ARM processor, it has been a trend that ARM processor can substitute the single-chip to realize data acquisition and control.

A new kind of remote I/O data acquisition system based on embedded ARM platform has been researched and developed in this paper, whose hardware platform use 32-bit embedded ARM microprocessor, and software platform use the Micro/OS-II core of real-time multitask operating system which is open-source or a stored program control for minor sensing operations. This system can measure all kinds of electrical and thermal parameters such as voltage, current, thermocouple, RTD, and so on.

The measured data can be displayed on LCD of the system, and at the same time can be transmitted through RS485 or Ethernet network to remote

DAS or DCS monitoring system by using Modbus/RTU or Modbus/TCP protocol.

The system has the dual redundant network and long-distance communication function, which can ensure the disturb rejection capability and reliability of the communication network.

Design of Key Expander for 128-bit AES algorithm

Bindu Madhavi G, M. Gowthami, N. Ushashree

Abstract

Advanced Encryption Standard (AES) is used nowadays extensively in many network and multimedia applications to address security issues. Transmission and storage of sensitive data in open networked environments is rapidly growing. Along with it, grows the need of efficient and fast data encryption. Software implementations of cryptographic algorithms cannot provide the necessary performance when large amounts of data have to be moved over high-speed network links that reach the Gbps range. Therefore hardware implementations have to be considered for these applications, either in the form of ASIC or FPGA designs. FPGAs are very well suited for high-speed cryptography, as they can provide the required performance.

The AES algorithm is a round-based, symmetric block cipher. It processes data blocks of fixed size (128 bits) using cipher keys of length 128, 196 or 256 bits. Depending on the key used, it is usually abbreviated as AES-128, AES-196 or AES-256 respectively. In this project only AES-128 is considered, as it is the most popular variant of the algorithm. The functional blocks of the algorithm are Key expansion and encryption. The initial 128-bit cipher key has to be expanded to new eleven round keys of same length. In order to produce a new round key, two transformations have to be performed, RotWord and SubWord.

The overall System Architecture will be designed using HDL language and simulation, synthesis and implementation (Translation, Mapping, Placing and Routing) will be done using various FPGA based EDA Tools.

CAN Based Accident Avoidance System

D. Madhura Sukanya, S. K. L. Prasad

Abstract

The main aim of this project is to avoid accidents based on CAN protocol by using AT89S52 programmable microcontroller.

CAN is a multi-master broadcast serial bus standard for connecting electronic control units (ECUs).Each node is able to send and receive messages, but not simultaneously: a message (consisting primarily of an ID usually chosen to identify the message-type/sender and up to eight message bytes) is transmitted serially onto the bus, one bit after another this signal pattern codes the message (in NRZ) and is sensed by all nodes.

The devices that are connected by a CAN network are typically sensors and control devices. In this project we are using CAN protocol to avoid accidents in automobiles. Basically, CAN protocol is used for the data transfer between different nodes.

In this project we are using ultrasonic sensor, connected either front side or backside to find the distance between the vehicle and obstacle and data transferring and controlling of various sensors will be performed based on CAN Standards .

Design of slave I2C bus Controller

V L.Apurva Swathi, B. Kruthika

Abstract

I2C(Inter Integrated Circuit) Bus is a two wire, low to medium speed communication bus that is used to attach low-speed peripherals to Mother board, Embedded system or cell phone. I2C was created to reduce the manufacturing cost of Electronic Products. It provides a low-cost, but powerful chip-to-chip communication link within these Electronic products.

Earlier chip-to-chip -communications use many wires in a parallel interface But I2C performs chip-to-chip communications using only two-wires clock (SCL) and data(SDA) in a serial interface, allowing I2C communicate with fewer pins(2 only).SDA carries data while SCL synchronizes sender and receiver during transfer. Thus, reducing size and cost of IC's and PCB's based on I2C Bus. Thus, we can say that I2C is a low cost, Powerful, Time proven, Industry standard, communication protocol used in wide variety of electronic products.

The overall system Architecture will be designed using HDL Language & simulation, synthesis and implementation(Translation, Mapping, Placing and Routing) will be done using various FPGA based EDA tools. Finally, the proposed system Architecture Performance (Speed, Area, Power and throughput) will be compared with already existing system implementation.

Design Of Multi-Lane Pci-Xp Physical Layer Transmit Protocol

S. Harika, S. Udayasri, Badam Varsha

Abstract

PCI Express is a 3rd generation high performance I/O bus used to interconnect peripheral devices in applications such as mobile, desktop, workstations, server, embedded computing and communication platforms. PCI Express implements switch-based technology to interconnect a large number of devices. Communication over the serial interconnect is accomplished using a packet based communication protocol. Physical layer link could be configured varying from 1 32 lanes, with each lane carrying a max data rate of 2.5Gbits/sec.

PCI Express protocol follows a layered structure similar to the OSI model and contains the following four layers: Software Layer, Transaction Layer, Data Link Layer, and Physical Layer. The project deals with the Design of Multi (four) lane Physical Layer Transmit Protocol, which connects to the Link on one side and connects to the Data Link Layer on the other side. It essentially process packets arriving from the Data Link Layer, and then converts them into serial bit stream.

The physical layer frames the packet with start and end of packet bytes before lane striping, byte scrambling to reduce electromagnetic emissions (EMI), and 8b/10b encoding to ensure sufficient transitions for clock and data recovery, and serialization of the 10-bit symbols before transmission across the link to the receiving device. The packet traverses up the protocol stack at the receiving device until data is extracted and passed to the device core.

A Voice Activated Robo Based On Dtmf

Rayalla Kowsalya, Pagilla Nagaraju, Gaddasu Rohini Priyan

Abstract

The proposed research work presents a systematic approach to design and implement a Voice-Activated Programmable Robot based on a low power, 8-bit AT89S52 microcontroller, remotely operated by the use of DTMF technology. It has a voice assistance feature so all the information about an organization can be recorded and played back for guiding the visitors in an organization or blind people. Time based event management can be carried out, as it is equipped with a Real Time Clock.

Dual-tone multi-frequency signaling (DTMF) is used for telecommunication signaling over analog telephone lines in the voice-frequency band between telephone handsets and other communications devices and the switching center. The version of DTMF that is used in push-button telephones for tone dialing is known as Touch-Tone. The APR9600 device offers single chip voice recording, non-volatile storage and playback capability for 40 to 60 seconds. It has a microphone interfacing for storing the incoming voice signals and during playback the stored signals are retrieved and then amplified before being fed to an external speaker.

This proposed work would be implemented using embedded design methodology, which includes Embedded hardware and firmware design modules. This project would be carried out with AT89S52 Micro controller, industry driven Embedded EDA Tool kits and Embedded 'C' Language.

Design and Implementation of 32-Bit RISC Processor

D Vijay Kumar, Thangalapally Ramesh, Pabbala Suman

Abstract

The RISC must use simple constructs and have small instruction set compared to CISC Processors. It is basically designed in order to achieve faster executions. The striking feature of RISC is that, it executes each instruction within one clock cycle. This is achieved carrying out most of the operation with in the Processor and minimizing the use of frequent operations requiring slower peripherals. Its architecture simplifies the instruction set and encourages the optimization of register manipulation. Almost all instructions have simple Register addressing. An important aspect of the instruction set is that it is easy to decode (Fixed length instruction format). Thus the Opcode and Instruction Register fields can be accessed simultaneously.

This RISC processor is designed to incorporate 20 basic instructions involving Arithmetic, Logical, Data Transfer and Control instructions. To implement these instructions the design incorporates various design blocks like Control Logic Unit (CLU), Arithmetic Logic Unit (ALU), Accumulator, Program Counter (PC), Instruction Register (IR), Memory, Clock Generator, Resister and additional glue logic. The Instruction format contains first four MSB bits as OPCODE and remaining 28bits as Address bus. It can address 256Gbytes of memory locations and 32-bit Bi-directional Data Bus.

Design and implementation of a Field programmable CRC Circuit architecture

Anudeep. I, Divya Surabhi, B. Chandra Shekar Yadav

Abstract

Cyclic redundancy check (CRC) is an error detecting code that is widely used to detect corruption in blocks of data that have been transmitted or stored. Hardware configurability that will allow unrestricted CRC sizes and polynomials to be deployed enables a wide range of network transmission, storage and security application.

In this research work, we derive a fully field programmable, parallel architecture for CRC computation circuit. The objective was to explore a domain specific programmable architecture capable of supporting high-speed line rates at a minimal area cost. The resulting architecture is able to support all types and sizes of CRC polynomials, for all types of protocols and data encryption. The architecture has been designed to be field programmable so that it is fully flexible in terms of the polynomials deployed and the input port width. The circuit includes an embedded configuration controller that has a low reconfiguration time and hardware cost. Data integrity is imperative for many network protocols, especially data-link layer protocols. Techniques using parity codes and hamming codes can be used for data verification, but CRC is preferred and most efficient method used for detecting bit errors produced from medium related noise.

The over all System Architecture will be designed using HDL language and simulation, synthesis and implementation (Translation, Mapping, Placing and Routing) will be done using various FPGA based EDA Tools. Finally the proposed system architecture performance (speed, area, power and throughput) will be compared with already exiting system implementations.

Microcontroller Based Arinc 429 Bus Controller

J.Premsagar, D.Asheervadham

Abstract

The project involves design and development of an ARINC 429 data bus controller. A microcontroller (Intel 87C51) will be interfaced to an ARINC 429 device(HI-8582).This interface will be useful for the transmission of digital data as per the format of ARINC 429 standard, between any two avionic equipments.

ARINC specification 429 also known as Mark 33 Digital information Transfer System (DITS) is a standard that is widely used in avionics industry for the transfer of digital data between avionics system elements. The ARINC 429 specification replaces the earlier ARINC 419 specification and was developed to alleviate much of the previous confusion by defining the standard for a single form of serial transmission.

ARINC 429 requires that the digital data is transmitted as a differential signal over a unidirectional bus composed of two twisted and shielded wires. All flight functions have been assigned a particular data or data format by the specification in order to prevent conflicts.

The ARINC 429 specification eliminates the need for complex interfaces between avionics systems produced by different manufacturers and provides a certain amount of plug in compatibility and universality.

The ARINC 429 Interface device (HI-8582) is used for interfacing a 16-bit parallel data bus directly to the ARINC 429 serial bus. The data bus and all control signals are CMOS and TTL compatible. Timing based on 1MHz clock.

Design and implementation of a Field programmable CRC Circuit architecture

Rayalla Kowsalya, Pagilla Nagaraju, Gaddasu Rohini Priyan

Abstract

This project deals with the design and simulation of 32-bit floating point basic arithmetic unit for RISC/DSP processor applications. It is capable of representing real and decimal numbers. The floating operations are incorporated into the design as functions. The numbers in contention have to be first converted into the standard IEEE floating point standard representation before any sorts of operation are conducted on them. The floating representation for a standard single precision number format is 32-bit number that is segmented to represent the floating point number.

The IEEE format consists of three fields, one bit for the sign. The next eight bits are that of exponent magnitude, and the remaining 23-bits represent the mantissa and mantissa sign. The exponent in this IEEE standard is represented in excess-127 format multiplication will be implemented by the processor. The main functional blocks of floating point arithmetic processor design includes arithmetic logic unit (ALU), register organization, control and decoding unit, memory block, 32-bit floating point basic arithmetic unit. This processor IP core can be embedded at many places such as co-processor for embedded DSP and embedded RISC controller.

The overall system architecture will be designed using HDL language and simulation, synthesis and implementation(translation,mapping ,placing and routing) will be done using various FPGA based EDA tools. Finally in the proposed system architecture performance (speed, area, power and throughput) will be compared with already existing system implementations

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Performance of grid connected Photo Voltaic (PV) system for different loads

V.Bharath Kumar , P.Shashank, V.Sai Ganesh, P.H.Yamini

Abstract

Demand for electricity is increasing at rapid rate, but using conventional fuels for generation power is cause for increase pollution. The resources are limited with conventional fuel systems. In order to overcome this kind of problems now a day's we are choosing non conventional sources, such as solar, wind for the production of power.

Solar energy is most important due to its continuous availability, so now a day's solar based power generation technologies are developing by using advanced technologies. Photo voltaic cell is the basic element to get power using solar energy. Generally this kind of systems is preferred to operate as standalone systems.

In order to supply power to the distribution network these types of systems should be synchronized with the power grid. This project deals with the grid connection of PV system with distribution system the system performance will be estimated for different types of loads (RLC load, Motor load, rectifier load) and output is compared

The complete process of proposed system will be carried out in the environment of MATLAB/SIMULINK, which is powerful tool to solve the problems in electrical engineering.

REMARKS:

This project deals with utilization of non conventional energy resources which is the need of the day.The main idea of this project is to integrate the PV system to the grid and to test the response of the system when it is interfaced with different types of loads. Further we can extend this work to investigate the effect of the severity of PV power fluctuations on the life time of the battery storage system.

Modeling and Simulation of Permanent Magnet Synchronous Motor Drive system

C.Pranav, G.Sandeep, M.Mallikarjun, V.Swathi Kumar

Abstract

The Project deals with the detailed modeling of a permanent magnet synchronous motor drive system in Simulink. Field oriented control is used for the operation of the drive.

The simulation includes all realistic components of the system. This enables the calculation of currents and voltages in different parts of the inverter and motor under transient and steady conditions. The losses in different parts are calculated, facilitating the design of the inverter. A closed loop control system with a Proportional Integral (PI) controller in the speed loop has been designed to operate in constant torque and flux weakening regions.

Implementation has been done in Simulink. A comparative study of hysteresis and Pulse Width Modulation (PWM) control schemes associated with current controllers has been made in terms of harmonic spectrum and total harmonic distortion. Simulation results are given for two speeds of operation, one below rated and another above rated speed.

Remarks:

This simulation helps in developing new systems including motor drives by reducing cost and time because it uses permanent magnet instead of electromagnet, and thus facilitating the development of new systems.

Dynamic Performance Evaluation of DFIG Architecture for Wind Power Generation using MATLAB

Neha Gaikwad, P. Vineetha, S. Santhosh kumar, P. Sunil Kumar, M. Rohit

Abstract

Wind power is a popular form of the renewable energy sources and has been proved as potential source for electricity generation with minimal environmental effects. Modern wind farms can produce a sustainable amount of power, which can supplement the base power generated by thermal, nuclear, or hydro power plants, when they are integrated into the grid. Any loss of wind generation leads to severe stability problems and possibly cascade outage may take place. To integrate these large wind farms into the grid, the performance of the grid connected wind farms is required, in both steady state and transient conditions. Most of the modern large wind power plants utilize doubly fed induction generators.

The present work utilizes the sixth order mathematical model of grid connected doubly fed induction generator and conventional decoupled vector control techniques have been used for the controller designs. The response of the doubly fed induction generator wind turbine system to grid disturbances is simulated. Small signal studies have been presented on the considered system, in order to identify and quantify the cause of problem. Simulation results show that, the conventional doubly fed induction generator suffers from poor regulating characteristics during abnormal conditions.

Further, modifications to conventional architecture and controllers have been proposed to improve the performance. Voltage sag ride-through capabilities and small signal studies of the proposed wind turbine architectures have been investigated through simulations. It is observed that the proposed modifications to the architecture and controllers, give better performance than the conventional architecture in terms of damping.

Remarks:

The present work utilizes the sixth order mathematical model of grid connected doubly fed induction generator and conventional decoupled vector control techniques have been used for the controller designs. Modifications to conventional architecture and controllers have been proposed to improve the performance.

Total harmonic distortion using Z-Source inverter

Chaitanya K.N.K, D. Nagaraju, M. Anusha, D. Sevya, L.Sowjanya,

Abstract

This project titled "Total harmonic distortion using Z-Source inverter" presents a two level ac-dc-ac Z-source converter with output voltage buck-boost capability. A Z-source inverter system and control for adjustable speed drives (ASD). The Z-source inverter employs a unique LC network to couple the inverter main circuit to the diode front end. By controlling the shoot-through duty cycle, the Z-source can produce any desired output ac voltage, even greater than the line voltage. As results, the new Z-source inverter system provides ride-through capability under voltage sags, reduces line harmonics, and extends output voltage range. Simulation results will be presented to demonstrate the new features.

Remarks:

By using Z-source convertor the harmonic content of output is less when compared to the harmonic content of the output using traditional invertors.

Transient Stability Improvement Using Thyristor Controlled Braking Resistor

D.Mallesh, B.Prasanna Kumar Goud, T.Raghuvaran Reddy, K.Amar

Abstract

Power system is subjected to sudden changes in load levels. Stability is an important concept which determines the stable operation of power system. In general rotor angle stability is taken as index, but the concept of transient stability, which is the function of operating condition and disturbances deals with the ability of the system to remain intact after being subjected to abnormal deviations. A system is said to be synchronously stable (i.e., retain synchronism) for a given fault if the system variables settle down to some steady-state values with time, after the fault is removed.

For the improvement of transient stability the general methods adopted are fast acting exciters, circuit breakers and reduction in system transfer reactance. The modern trend is to employ FACTS devices in the existing system for effective utilization of existing transmission resources. These FACTS devices contribute to power flow improvement besides they extend their services in transient stability improvement as well.

Dynamic braking resistor is a very effective devise for transient stability control. In this project makes use of fuzzy logic controller for the switching of the thyristor controlled braking resistor to improve power system transient stability. The braking resistor installed at generator bus, where rotor speed of the generator is measured to determine the firing angle of the thyristor switch. By controlling the firing angle of the thyristor, braking resistor controls the accelerating power in generators and thus improves the transient stability.

Remarks:

FACTS controllers like TCBR, the one proposed helps in controlling the accelerating power in generator since power systems are non linear ,conventional fuzzy controller performs well in maintaining the power systems stability.

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Development of a process mapping tool

Karthik Siddavaram

Abstract

A process is a series of related activities which ensure proper functioning of any system in an organization. It is one of the most important components in a daily routine of a successful organization. The importance of identifying the key process participants and classifying them based on their functionality originates the need of process mapping. Process mapping is a path which allows in understanding, analyzing and documenting the processes and activities in an organization to identify the possible opportunities for improvement of an organization. This requirement can be addressed by development of a process mapping tool which maps the process to its functions keeping in view of the requirements of a system and classifying the process accordingly based on its functionality.

Problem Statement:

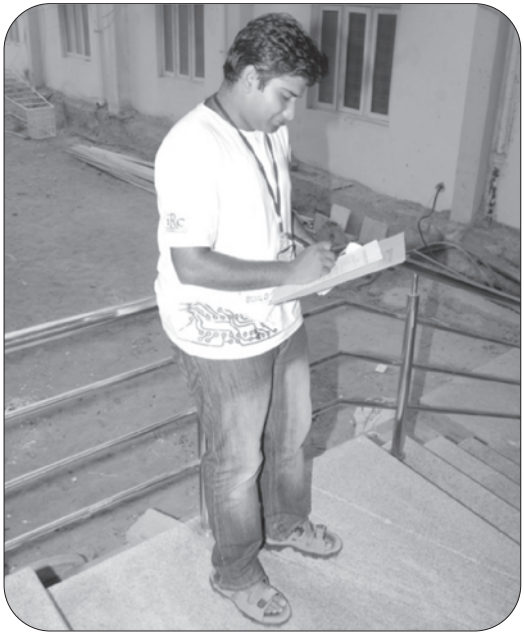
Development of a tool which maps process to its functions keeping in view of the requirements of a system.

Procedures:

Identifying the process participants based on their functionality. Classifying these processes into sub process to facilitate efficient functioning of a system.

Results:

Internal tool for Tata Consultancy Services.



Supply Chain

C.Pranav, G.Sandeep, M.Mallikarjun, V.Swathi Kumar

Abstract

Supply chain is the management of a network of interconnected businesses involved in the ultimate provision of product required by the end customers. Supply chain spans all movement and storage of materials, goods from point of origin to point of consumption (supply chain). And also defines SC as the design, planning, execution, control and monitoring of supply chain activities with the objective of creating net value, building a competitive infrastructure, leveraging worldwide logistics, synchronizing supply with demand and measuring performance globally.

Problem Statement:

Development of a tool which monitors supply chain keeping in view of the requirements of a system.

Result:

Internal tool for Electronics Corporation of India Limited.

Transperant Evaluation System Using Ms Azure

Tejas D. Gosar, Akhil Gowd, Nithun reddy

Abstract

Today universities are growing with more and more affiliated colleges getting added every year. With increased students the evaluation system is becoming extremely difficult to manage. Today the marks are declared and lot of students are unhappy with this closed system as there is no way to understand their actual performance. Most of the times in experienced faculty evaluate the papers. Students apply for recounting and again have no idea if their papers were really looked into.

The purpose of the project is to create an Evaluation system model that authenticates the user and facilitates the authorized user to view the answer paper and the revaluated mark sheet on the server. Using Windows Azure we deploy the application on the cloud. The SQL Azure provides us with a way to store and retrieve data from a central location which makes the application easy to update the data.

An Adaptive Programming Model For Fault-Tolerant Distributed Computing

N.Goutham, S.Jagdish, Sashi Kumar

Abstract

The capability of dynamically adapting to distinct runtime conditions is an important issue when designing distributed systems where negotiated quality of service (QoS) cannot always be delivered between processes. Providing fault tolerance for such dynamic environments is a challenging task. Considering such a context, this paper proposes an adaptive programming model for fault-tolerant distributed computing, which provides upper-layer applications with process state information according to the current system synchrony (or QoS).

The underlying system model is hybrid, composed by a synchronous part (where there are time bounds on processing speed and message delay) and an asynchronous part (where there is no time bound). However, such a composition can vary over time, and, in particular, the system may become totally asynchronous (e.g., when the underlying system QoS degrade) or totally synchronous. Moreover, processes are not required to share the same view of the system synchrony at a given time. To illustrate what can be done in this programming model and how to use it, the consensus problem is taken as a benchmark problem. This paper also presents an implementation of the model that relies on a negotiated quality of service (QoS) for communication channels.

Spatio-Temporal Network Anomaly Detection By Assessing Deviations Of Empirical Measures

Phanitej M V S, Siddarth Kalia, Sravan Kumar P

Abstract

We introduce an Internet traffic anomaly detection mechanism based on large deviations results for empirical measures. Using past traffic traces we characterize network traffic during various time-of-day intervals, assuming that it is anomaly-free. We present two different approaches to characterize traffic: (i) a model-free approach based on the method of types and Sanov's theorem, and (ii) a model-based approach modeling traffic using a Markov modulated process. Using these characterizations as a reference we continuously monitor traffic and employ large deviations and decision theory results to “compare” the empirical measure of the monitored traffic with the corresponding reference characterization, thus, identifying traffic anomalies in real-time. Our experimental results show that applying our methodology (even short-lived) anomalies are identified within a small number of observations. Throughout, we compare the two approaches presenting their advantages and disadvantages to identify and classify temporal network anomalies. We also demonstrate how our framework can be used to monitor traffic from multiple network elements in order to identify both spatial and temporal anomalies. We validate our techniques by analyzing real traffic traces with time-stamped anomalies.

Cloud Based Game Management System

Priyank V W, Tarun Poddar

Abstract

A cloud is a virtual space available for the users to deploy their applications. A cloud service has three distinct characteristics that differentiate it from traditional hosting.

It is sold on demand, typically by the minute or the hour; it is elastic- a user can have as much or as little of a service as they want at any given time; and the service is fully managed by the provider (the consumer needs nothing but a personal computer and Internet access).

Significant innovations in virtualization and distributed computing, as well as improved access to high-speed Internet and a weak economy, have accelerated interest in cloud computing.

If you design a web portal for a Game, you understand the challenges of managing IT. A clear solution for building and managing an infrastructure suited to the new is cloud-based computing.

Building your own infrastructure to handle peak volume requires capital investments and no matter how big you build it, it still may not be enough.

Cloud-based computer resources and sophisticated management platforms, on the other hand, can deliver increased flexibility and lower costs for large traffic events and ongoing lifecycle management. Once your application is running you will have full automation and expert management for large volume, highly-elastic.

Managing Gps Rinex Data For Crustal Deformation Studies

K.Bhasuri, S.Indraja

Abstract

Crustal deformations takes place every moment. Continuous monitoring of crustal deformation can give an insight into the various phases of the earthquake cycle. This in turn provides the earth scientists with the knowledge required for forecasting earthquakes and provide warnings about seismic risk.

During these observations, the raw data produced is converted into RINEX(Receiver INdependent EXchange) format. Data is collected on daily basis with an interval of 30 seconds in four major regions in INDIA. All the stations present in these regions are about 60 in number which are uniquely distinguished by a four character station codes.

In this project, an authorized user can upload a desired or missing file into the data base. The data files present in database can be viewed according to stations present or by specified interval of julian bandwidth (starting and ending dates) which can also be downloaded. Apart from it, this project also allows authorized user to view and make changes into the data file which is already existing in database. The user can also view the list of files available in a station with specified 4 character station code with the help google maps integrated here and download it too.

Student Project Allocation And Management With Online Testing System

T.Naga Padmini, K.Madhulatha, V.Surekha

Abstract

This project is aimed at developing a web-based system, which manages the activity of "Student Project Management" and "Online Testing". This system will manage the database and maintain a list of all student groups that have registered on this site, conduct their online test and shortlist those students who have passed the eligibility criteria as set by the professors.

This is a system used by Educational Institutions or other organizations, which are willing to give student projects. We have three roles in this system, an administrator, a professor and a student. An administrator logs into this system, and can register a professor who belongs to that institution.

Students register in this system and get userid. A student should register, provide his information (like semester marks, technologies familiar with, prior project experience etc.,) and also provide information about his team members. This is saved in a database.

In the same system the professors who have been registered by the administrator can login and then shortlist students by their academic performance (percentage as entered by the students during their registrations) and/or test score.

Controlling Pc Using Mobile Application

S.Ankita, G.Swathi, A.Pushpak Reddy

Abstract

The flow of work in this application is manual in nature which involves a mobile acting as a client controls the PC through a Wi-Fi network provided with the same DNS for the mobile and the PC connected.

First the server, PC, is initialized by giving a password to it. Then the mobile within the same WI-FI network is been initialized by giving some details of the PC which a user want to access (details like IP address, default port no, password provided same to that of password given in server).

After connection establishment using mobile we can access the complete PC through internet within the Wi-Fi network and we can perform operations like

1. Shutdown
2. Restart
3. Open items like notepad, WordPad, paint etc.
4. View file system
5. Cursor movements
6. Keyboard operations
7. View screen (with adjustable size).

DEPARTMENT OF INFORMATION TECHNOLOGY

Capturing Router Congestion and Delay

V.Anusha, A.Snigdha, R.S.L Priyanaka

Abstract

Using a unique monitoring experiment, we capture all packets crossing a (lightly utilized) operational access router from a Tier-1 provider, and use them to provide a detailed examination of router congestion and packet delays. The complete capture enables not just statistics as seen from outside the router, but also an accurate physical router model to be identified. This enables a comprehensive examination of congestion and delay from three points of view: the understanding of origins, measurement, and reporting.

Our study defines new methodologies and metrics. In particular, the traffic reporting enables a rich description of the diversity of micro congestion behavior, without model assumptions, and at achievable computational cost.

Design and build of research application

K.Krishnakanth Reddy, D.Ravi Shankar

Abstract

A fundamentall problem that underlies many important network functions such as QoS routing, path selection, and traffic engineering, is to find the constrained shortest path the cheapest path that satisfies a set of constraints. For interactive real-time traffic, the delay constrained least-cost path has particular importance . It is the cheapest path whose end to-end delay is bounded by the delay requirement of a time-sensitive data flow. The additional bandwidth requirement, if there is one, can be easily handled by a pre processing step that prunes the links without the required bandwidth from the graph.

The algorithms for computing the constrained shortest paths can be used in many different circumstances, for instance, laying out virtual circuits in ATM networks, establishing wavelength- switching paths in fiber-optics networks, constructing label-switching paths. There are two schemes of implementing the QoS routing algorithms on routers. The first scheme is to implement them as on-line algorithms that process the routing requests as they arrive.

In practice, on-line algorithms are not always desired. When the request arrival rate is high 1 To solve this problem, the second scheme is to extend a link-state protocol and periodically pre-compute the cheapest delay-constrained paths for all destinations, for instance, for traffic with an end-to-end delay requirement. The computed paths are cached for the duration before the next computation.

This approach provides support for both constrained unicast and constrained multicast. The computation load on a router is independent of the request arrival rate. Moreover, many algorithms, including those we will propose shortly, have the same time complexity for computing constrained shortest paths to all destinations or to a single destination. This paper studies the second scheme.

NGRI Attendance

K. Sarvani, K. Gayatri, V. Sai Krithi

Abstract

The domain objective of our project is to develop a data base management system that will be sued to assess the performance of the employees of NGRI.

It is a real time project that will be implemented in NGRI. The project basically contains 3 modules, in which the data is mined from the system files which is given as an input to this project from the presently operative biometric log-in log-out system.

The main aim of this project is to develop a user interface accessible by the administrator and generate performance reports of the employees. This includes manipulating the knowledgebase extracted from the data mining module and applying the performance evaluation criteria using J2SE and JSwing for user interface. Also the project uses a mailing system (JAVA mail) to generate automatic reports to the respective staff members who fall short of the attendance or who do not reach the performance criteria.

Computational Approach to estimate the relationship between reservoir water level and seicmicity of the region.

V.Anusha, A.Snigdha, R.S.L Priyanaka

Abstract

Using a unique monitoring experiment, we capture all packets crossing a (lightly utilized) operational access router from a Tier-1 provider, and use them to provide a detailed examination of router congestion and packet delays. The complete capture enables not just statistics as seen from outside the router, but also an accurate physical router model to be identified. This enables a comprehensive examination of congestion and delay from three points of view: the understanding of origins, measurement, and reporting.

Our study defines new methodologies and metrics. In particular, the traffic reporting enables a rich description of the diversity of micro congestion behavior, without model assumptions, and at achievable computational cost.

Mobility Management Approaches for Mobile IP Networks

S.Sri Priya, M.Madhavi, R.Jyothi

Abstract

In wireless networks, efficient management of mobility is a crucial issue to support mobile users. The Mobile Internet Protocol (MIP) has been proposed to support global mobility in IP networks. Several mobility management strategies have been proposed which aim reducing the signaling traffic related to the Mobile Terminals (MTs) registration with the Home Agents (HAs) whenever their Care-of-Addresses (CoAs) change. They use different Foreign Agents (FAs) and Gateway FAs (GFAs) hierarchies to concentrate the registration processes. For high-mobility MTs, the Hierarchical MIP (HMIP) and Dynamic HMIP (DHMIP) strategies localize the registration in FAs and GFAs, yielding to high-mobility signaling. The Multicast HMIP strategy limits the registration processes in the GFAs. For high-mobility MTs, it provides lowest mobility signaling delay compared to the HMIP and DHMIP approaches. However, it is resource consuming strategy unless for frequent MT mobility. Hence, we propose an analytic model to evaluate the mean signaling delay and the mean bandwidth per call according to the type of MT mobility. In our analysis, the MHMIP

Outperforms the DHMIP and MIP strategies in almost all the studied cases. The main contribution of this paper is the analytic model that allows the mobility management approaches performance evaluation.

Network Border Patrol: Preventing Congestion Collapse

G.Shilpa, R.Bhargavi

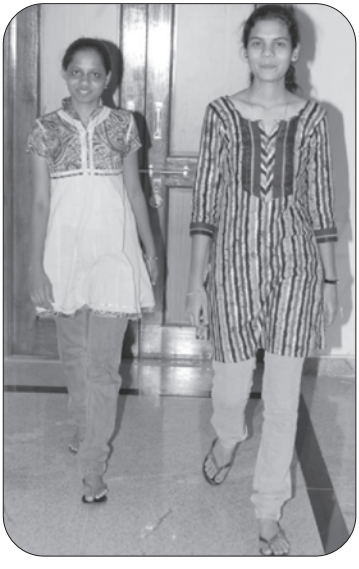
Abstract

The fundamental philosophy behind the Internet is expressed by the scalability argument: no protocol, mechanism, or service should be introduced into the Internet if it does not scale well. A key corollary to the scalability argument is the end-to-end argument: to maintain scalability, algorithmic complexity should be pushed to the edges of the network whenever possible.

Perhaps the best example of the Internet philosophy is TCP congestion control, which is implemented primarily through algorithms operating at end systems. Unfortunately, TCP congestion control also illustrates some of the shortcomings the end-to-end argument. As a result of its strict adherence to end-to-end congestion control, the current Internet suffers from main maladies: congestion collapse from undelivered packets.

The Internet's excellent scalability and robustness result in part from the end-to-end nature of Internet congestion control. End-to-end congestion control algorithms alone, however, are unable to prevent the congestion collapse and unfairness created by applications that are unresponsive to network congestion. To address these maladies, we propose and investigate a novel congestion-avoidance mechanism called network border patrol (NBP).

NBP entails the exchange of feedback between routers at the borders of a network in order to detect and restrict unresponsive traffic flows before they enter the network, thereby preventing congestion within the network.



A Geometric Approach to Improving Active Packet Loss Measurement(changed from ocr)

D.B.Saraswathi, G.Mohan Krishna, P.Sandeep , Jawahar

Abstract

Data Migration is the process of transferring data between storage types, formats, or computer system. Data migration is usually performed programmatically to achieve an automated migration, freeing up human resources from tedious tasks. It is required when organizations or individuals change computer systems or upgrade to new systems, or when systems merge (such as when the organizations that use them undergo a merger/takeover).

To achieve an effective data migration procedure, data on the old system is mapped to the new system providing a design for data extraction and data loading. The design relates old data formats to the new system's formats and requirements. Programmatic data migration may involve many phases but it minimally includes data extraction where data is read from the old system and data loading where data is written to the new system.

After loading into the new system, results are subjected to data verification to determine whether data was accurately translated, is complete, and supports processes in the new system. During verification, there may be a need for a parallel run of both systems to identify areas of disparity and forestall erroneous data loss.

Automated and manual data cleaning is commonly performed in migration to improve data quality, eliminate redundant or obsolete information, and match the requirements of the new system.

Database migration similarly, it may be necessary to move from one database vendor to another, or to upgrade the version of database software being used. The latter case is less likely to require a physical data migration, but this can happen with major upgrades. In these cases a physical transformation process may be required since the underlying data format can change significantly. This may or may not affect behavior in the applications layer, depending largely on whether the data manipulation language or protocol has changed - but modern applications are written to be agnostic to the database technology so that a change from Oracle to MySQL, DB2 or SQL Server should only require a testing cycle to be confident that both functional and non-functional performance has not been adversely affected

A Routing-Driven Elliptic Curve Cryptography Based Key Management Scheme for Heterogeneous Sensor Networks

P.Harika, M.Madhuri, B.Anitha

Abstract

In an olden research on sensor network security mainly considers homogeneous sensor networks, where all sensor nodes have the same capabilities. Research has shown that homogeneous ad hoc networks have poor performance and scalability. The many-to-one traffic pattern dominates in sensor networks, and hence a sensor may only communicate with a small portion of its neighbors. Most existing key management schemes try to establish shared keys for all pairs of neighbor sensors, no matter whether these nodes communicate with each other or not, and this causes large overhead. We propose a novel routing-driven key management scheme, which only establishes shared keys for neighbor sensors that communicate with each other. The performance evaluation and security analysis show that can provide better security with significant reductions on communication overhead, storage space and energy consumption than other key management schemes.

Remote Web Desk

M.Shashidhar, P.Rahul, B.V.Ranjit Kumar

Abstract

It consists mainly of “Remote Frame Buffer” protocol which is implemented by a server on the controlled host and a client on controlling host. Since it makes no assumptions About the content of frame buffer, it is highly portable and very light weight, being applicable even to embedded systems.RFB provides facilities to transfer the screen image (or frame buffers) rectangles and transfer these rectangles containing pixel values to remote user allowing the available participants to share the view and control of session simultaneously. On the other hand, it also accepts the user interaction events (e.g. key press, mouse button click etc) from real-time conferees and forwards the events to the remote session.

JavaDatabase Administrator

G Abhishek, Ch.Padmini

Abstract

Graphical user interfaces are so called because we use mouse to point at graphical objects such as windows, menus, icons, buttons and other tools on the screen these graphical tools all represent different types of commands the GUI enables us to issue commands to the computer by using visual objects instead of typing commands this is one of the key advantage of the Graphical User Interface it frees us from memorizing and typing text commands

This project aims to develop a web based application by which a easy-to-use front-end to the database can be provided where the user is Alleviated from the burden of writing queries.

- Properties Window
- Searching Feature for selected table, view, synonym or snapshot.
- Performing Data Definition Language (DDL)/Data Manipulation Language using menu.

Automation of Time-Table

D. Sai Sindhuri, P. Sai Mukesh, P.Pavan Kumar

Abstract

An Educational institution is set with a goal to serve the society and make the future of the nation secured by developing the skills and make the students ready for the future challenges.

If it has to achieve this goal the first thing that has to be set is how to manage the time which is widely known as time management.

In any organization time management plays a key role in achieving the goals for which the institution has taken birth.

For this the institution requires a vision with which they can manage the time.

For that the time table is the tool for the time management. So that the institution can set their vision on the goals for which they have established it.

That's the reason why all the educational institutions first set their energies on the preparation of time table.

Because time table acts like eyes for the organization so that they can concentrate on their goals.

Finance Management System

N.Saidarao, M.Papaiah

Abstract

The system mainly deals with the automation of the activities performed at Andhra Pradesh State Finance Corporation (APSFC), which issued various kinds of loans to their Customers and accepts monthly installments from them.

All the master information is gathered pertaining to the employees working in the organization, Industries to whom the loans are issued. Different types of loans available are designed and the interest rates applicable are set in the master tables.

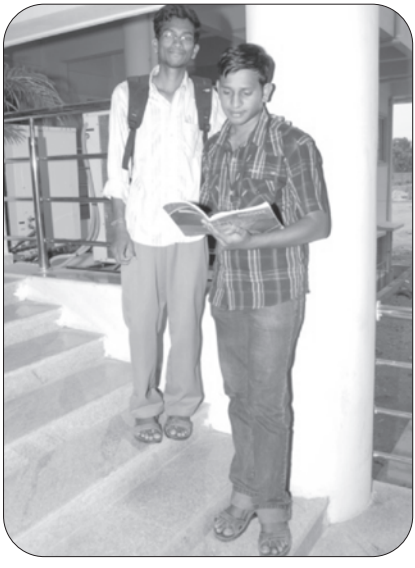
Initially after registering the customer, loan is sanctioned according to his requirement and eligibility. Details of a particular loan are gathered such as loan number, customer number, loan code, amount, interest, and number of months, monthly installment and date of sanction.

When the Industries pay the loan installments, details of loan number, payment id, amount and date of payment are gathered and stored.

Simply choosing the appropriate menus such as Employee details report, Customer details report, generates various reports, Loans detail report, Interest report, Customer-loan details report & Payment details report.

The system security is taken care of by a login form, which is allows only authorized users to utilize the system.

The main aim/objective is to develop an effective system, which is fast, accurate, consistent, reliable, and flexible enough so that in can accommodate any further expansion.



Automation of Interview Evaluation Details

Srikanth.G, Srikanth Varma.T

Abstract

The project is to automate the interview evaluation. The system will be developed at Polaris Software Labs Ltd., Hyderabad. The system can be used by the interview panel to automate the interview details. This project aims to automation process of capturing required data to generate the offer letters for the selected persons.

Modules:

1. Fresher 2. Experienced 3. H.R. 4. Referral 5. Project manager 6. Admin

Module Description:

Fresher:

This module is used to capture the candidate details while applying. Once this is done, the candidate can login and check the status.

Experienced:

This module is used to capture the candidate details and uploading of the CV also. Once this is done, the candidate can re-upload the CV. Once this is done, the candidate can login and check the status. The candidate will not able to modify the following details:

- PAN Card No • Passport No.
- Date of Birth

H.R:

A H.R can search for candidates according to his/her need. HR is provided with different search options, he/she can directly recruit candidates based on the company need. HR will either schedule or calls the candidate for interview. Once the candidate details are available and whenever the suitable position is available, the HR will change the status as follows:

Placements

VIGNANA BHARATHI INSTITUTE OF TECHNOLOGY

SYNTEL INC..

CAMPUS DRIVE ON 18th JAN 2011

VIGNANA BHARATHI INSTITUTE OF TECHNOLOGY

SERENE GLOBAL SERVICES

CAMPUS DRIVE ON 23rd JAN 2011

VIGNANA BHARATHI
Institute of Technology

(Approved by AICTE & Affiliated to JNT University)
Aushapur (V), Ghatkesar (M), R.R. Dist. - 501 301. A.P. India.
Ph : 08415-200419, 320
Visit us at:www.vbithyd.ac.in
E-mail : principal@vbithyd.ac.in